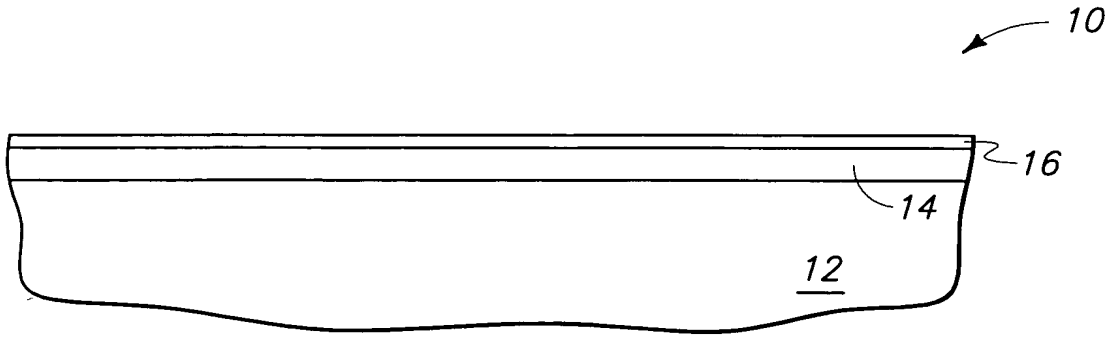


Fig 1

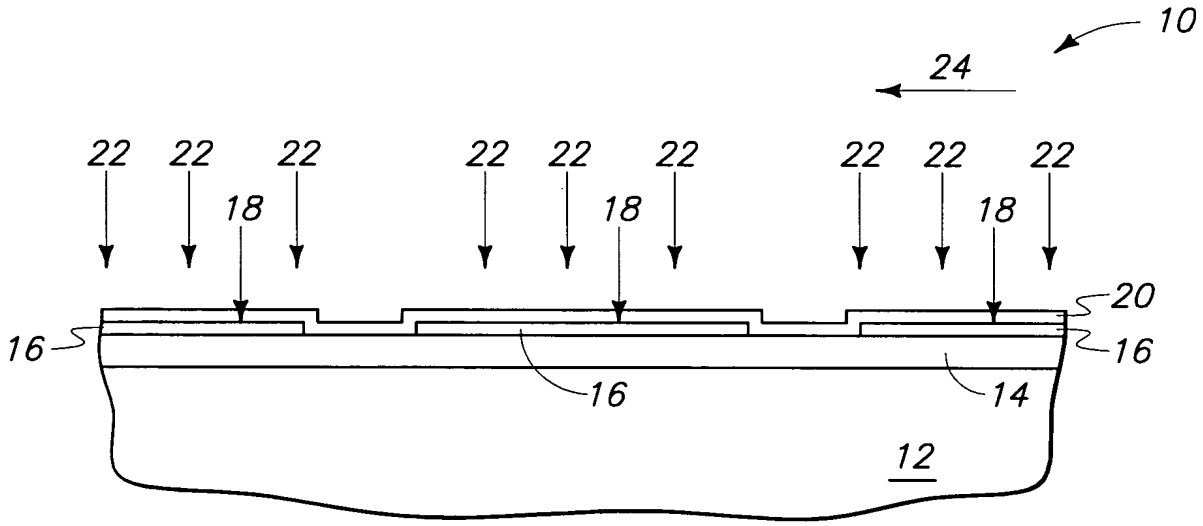


Fig 2

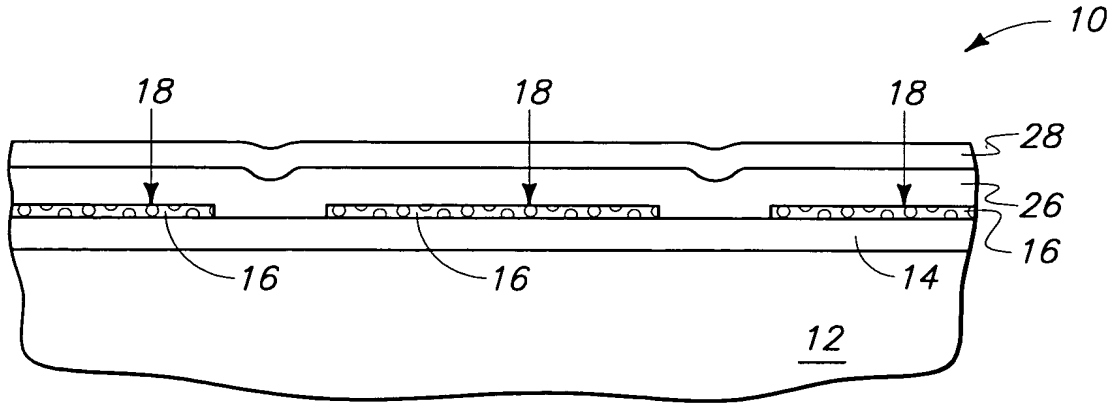


Fig 3

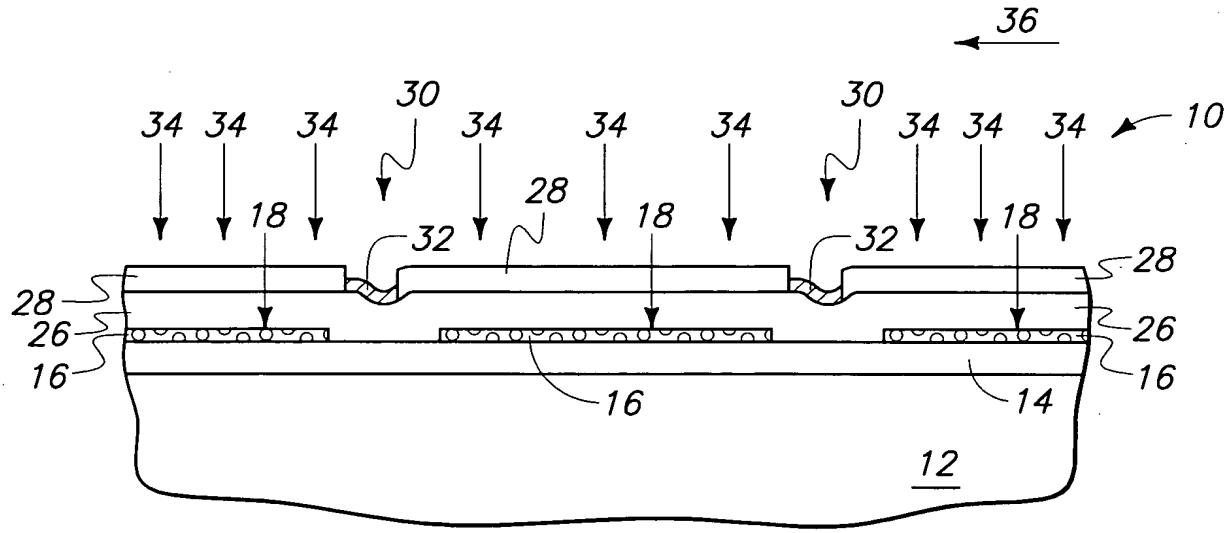


Fig 4

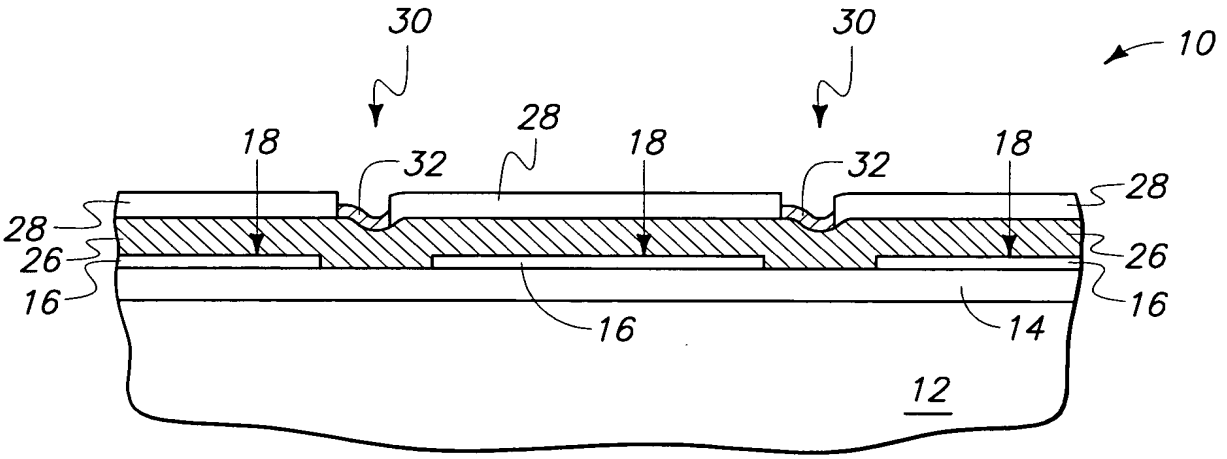


Fig 5

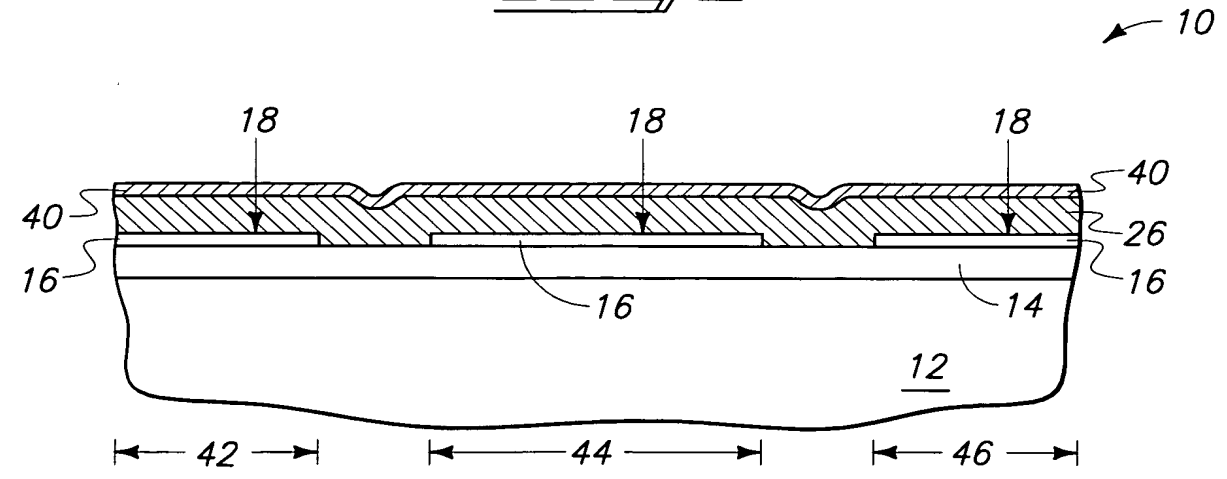
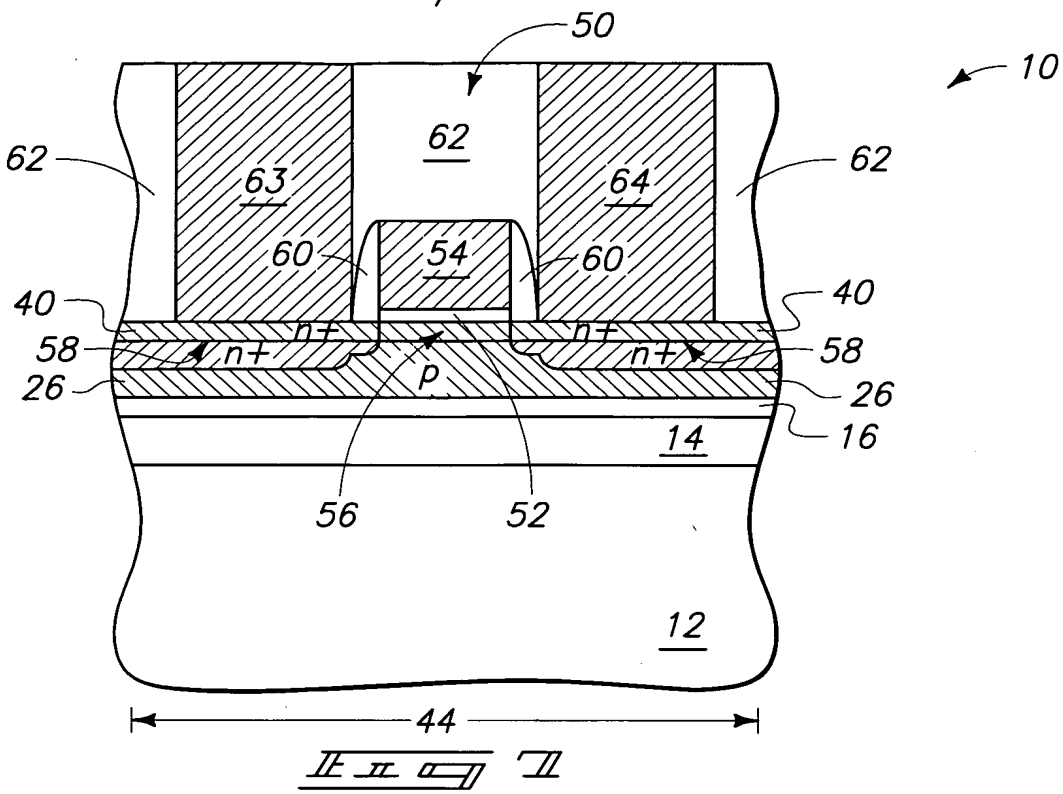


Fig 6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63
64
62
60
54
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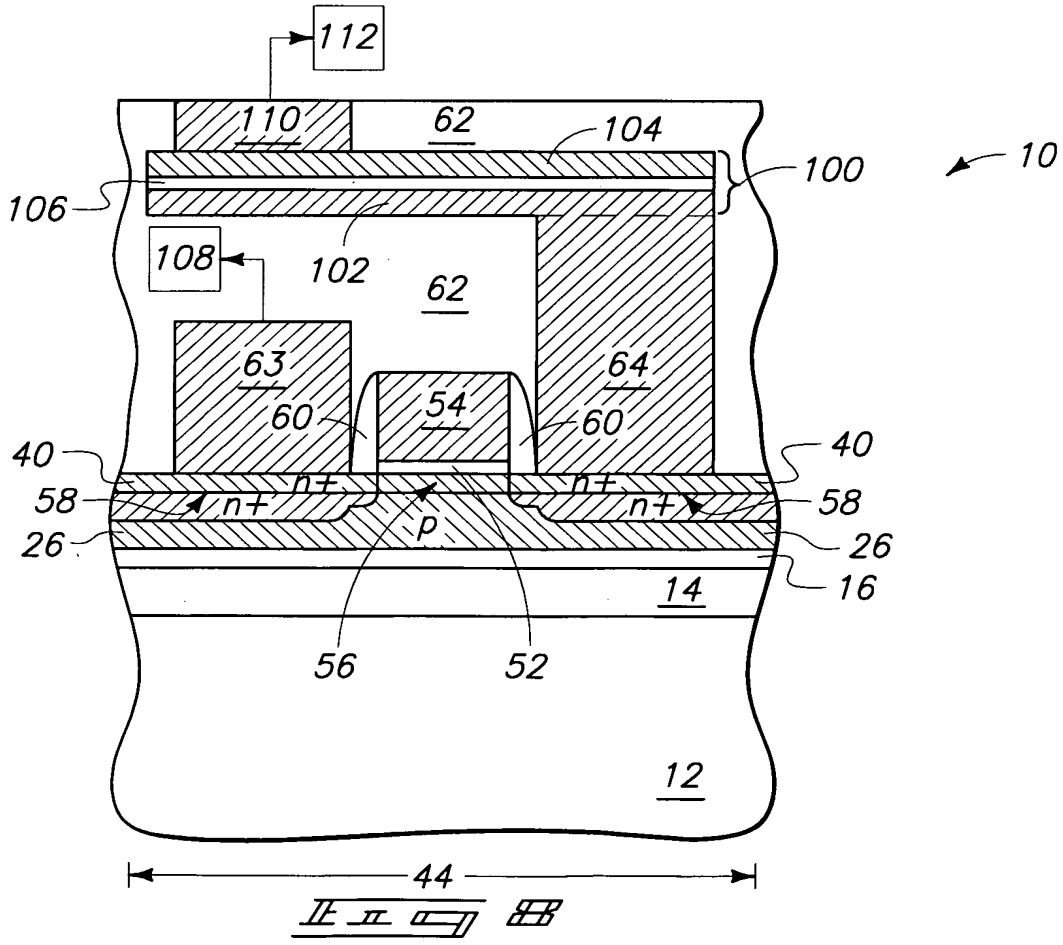
40
40
58
n+
n+
n+
58
26
p
26
16
14
56
52
12
44

FIG. 7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n+
n+
58
26
p
26
16
14
56
52
12
44

FIG. 8

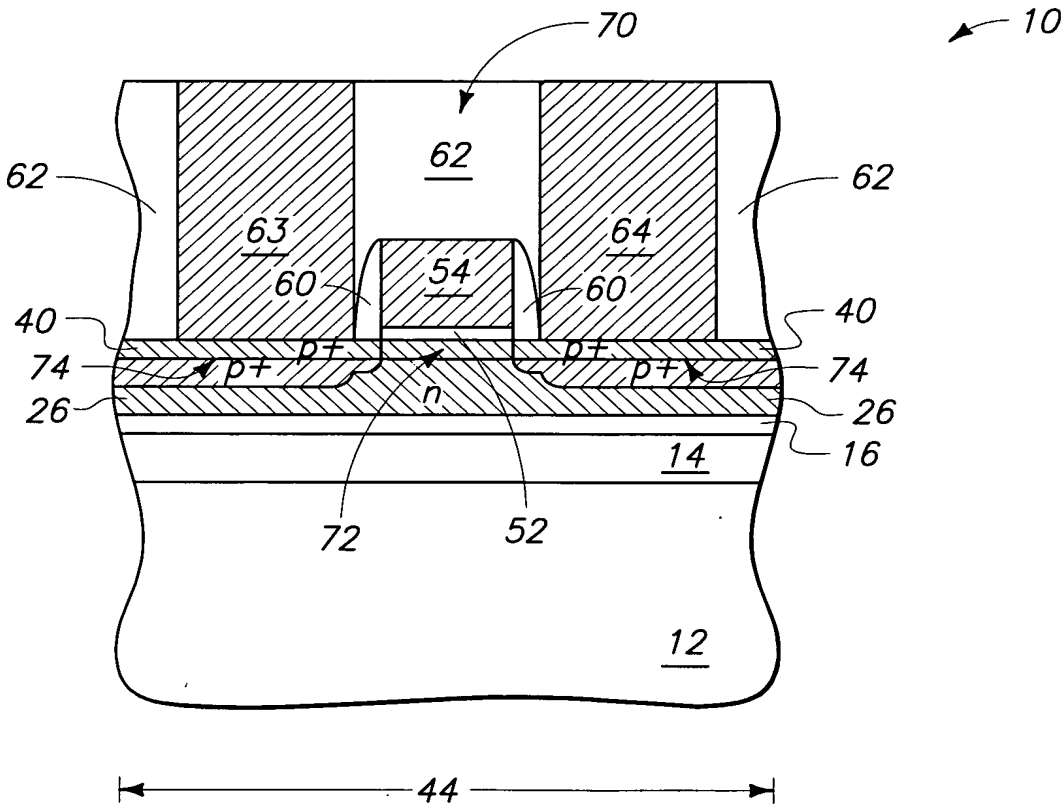
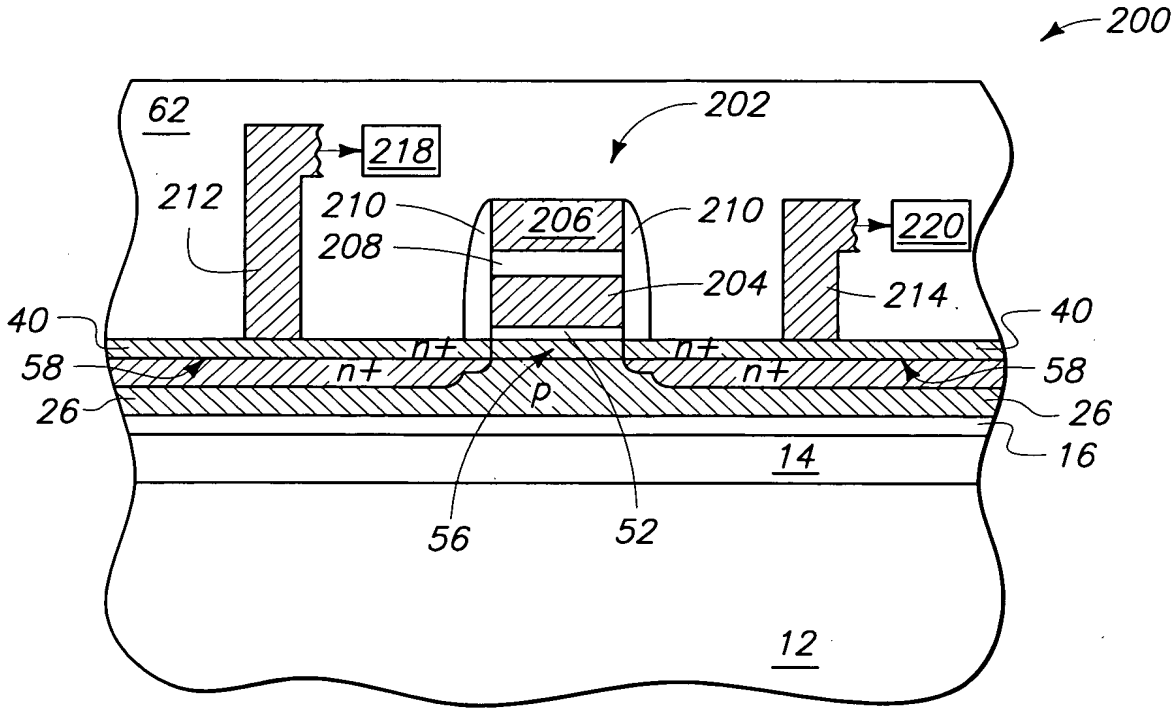


Fig. 9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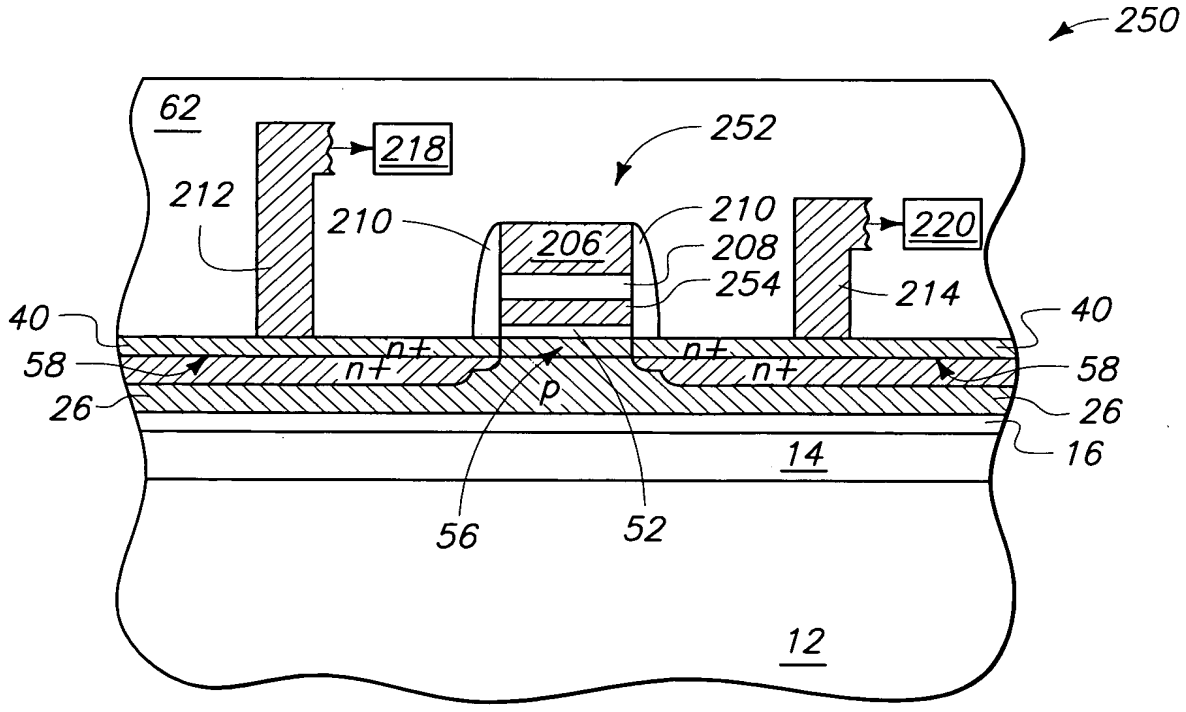
n+
n+
n+
58
p
26
26
14
16
56
52
12

Fig. 1B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n+
n+
n+
58
p
26
26
14
16
56
52
12

Fig. 2

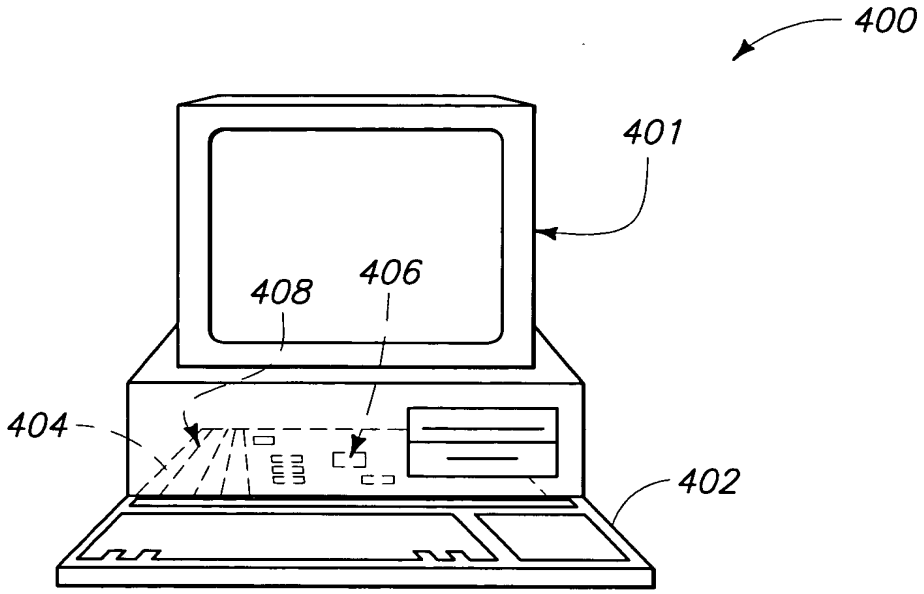


Fig 12

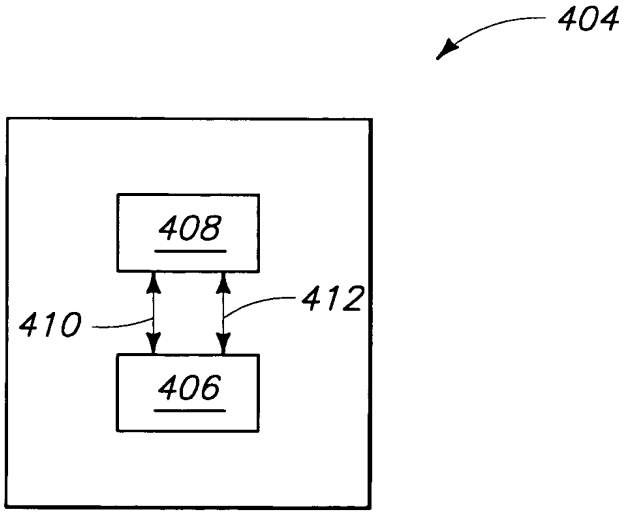


Fig 13

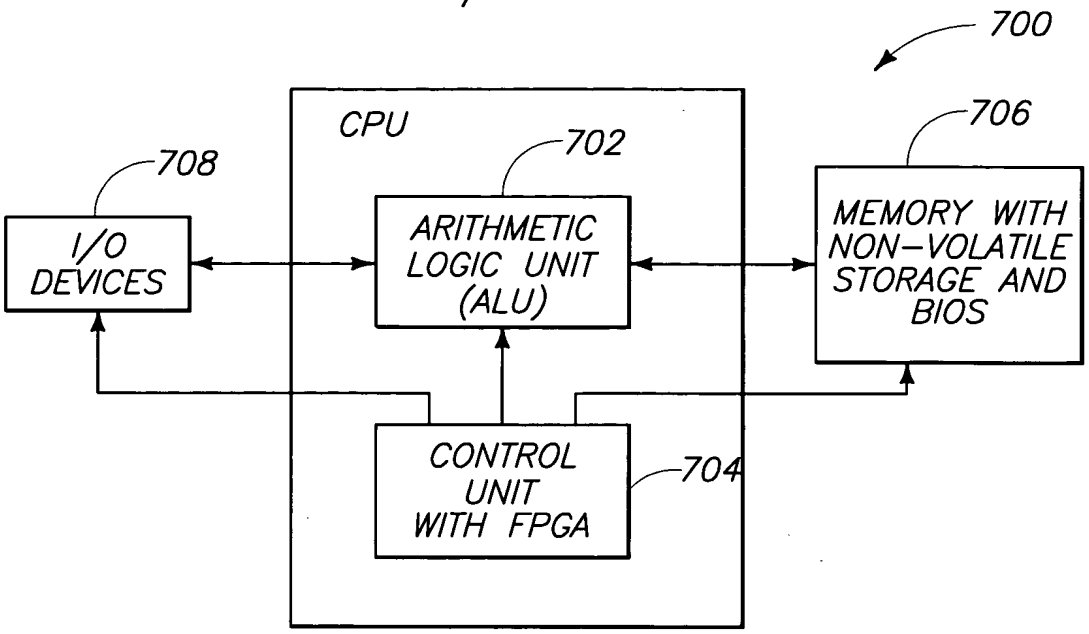
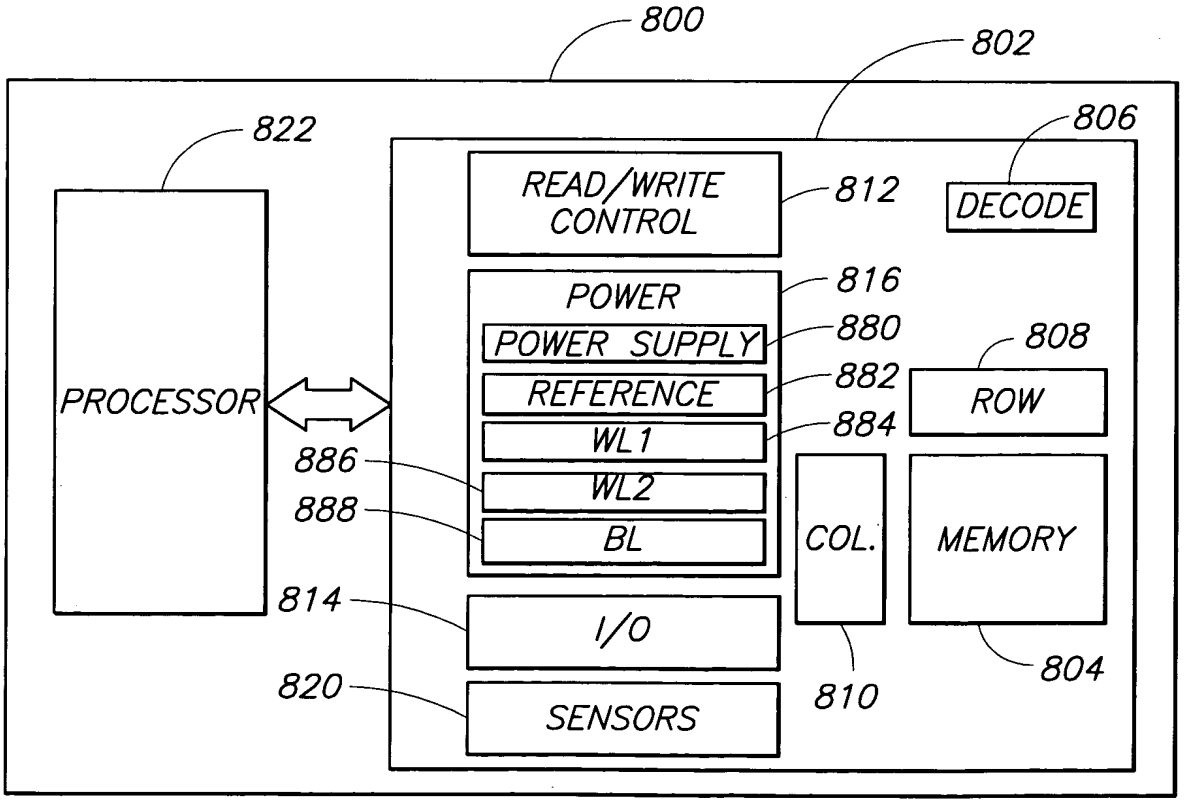

700
CPU
702
706
708
I/O DEVICES
ARITHMETIC LOGIC UNIT (ALU)
MEMORY WITH NON-VOLATILE STORAGE AND BIOS
CONTROL UNIT WITH FPGA
704

Fig 14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802
822
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READ/WRITE CONTROL
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DECODE
816
POWER
880
POWER SUPPLY
808
882
REFERENCE
ROW
PROCESSOR
884
WL1
886
WL2
888
BL
COL.
MEMORY
814
I/O
804
820
SENSORS
810

Fig 15